Experiment # 01

Introduction to Digital Logic Trainer and Familiarity with Logic Gates

Objective
Gaining familiarity with the use of digital trainer, exploring the different components of the trainer and familiarize students with the logic gates.

Apparatus
- Logic Trainer
- Wires
- Components (IC's)
- 74LS00
- 74LS02
- 74LS08
- 74LS32
- 74LS86

Theory
All experiments included in this manual shall been performed on the AM-2000 logic trainer. Before starting actual experiments; let us first familiarize our self with the use of AM-2000 trainer.

Measuring Power Supplies
Connect the AM-2000 Trainer to the 220V AC power source and turn ON the Trainer. Observe +5V, +12V, and -12V LED's ON, indicating these supplies are available for experimentation. Verify +5V, +12V and -12v voltages using a multi meter.

Measuring Logic Levels
Try using the LED's (L0-L15) to monitor the logic level.
1. Connect +5V power to the LED indicator L0. The LED should be ON indicating logic.
2. Connect LED indicator L0 to GND. the LED should be OFF indicating logic 0.

Test the Clock
Rotate the timer rate knob to counter clock wise position until extreme position is reached. Connect the output CLK to the input of LED L0.the light should blink ON and OFF slowly. The light blinks rapidly as the timer rate knob is rotated clock wise. It will stop blinking at some point and then LED will be ON indicating a higher frequency.

Measure the Logic Level Coming from One of the Logic Switch (S2 to S9):
Connect the outputs S2 AND S2' of switch (S2) to L0 and L1 respectively, The LED's should indicate the logic levels originating from the S2 switch.
1. Set switch S2 at a higher position, L0 should be OFF and L1 should be ON.
2. Set switch S2 at a lower position, L0 should be ON and L1 should be OFF.

BCD Logic Input

Connect switches S2, S3, S4 and S5 to the four-input marked as 8 4 2 1 on the SBB-63 board. Apply BCD input using switches, it would be decoded and displayed on the seven- segment display.

1. Set switch S2 at logic '1' and rest of the switches at '0', BCD digit '8' will be displayed.
2. Set switch S3 at logic '1' and rest of the switches at '0', BCD digit '4' will be displayed.
3. Set switch S4 at logic '1' and rest of the switches at '0', BCD digit '2' will be displayed.
4. Set switch S5 at logic '1' and rest of the switches at '0', BCD digit '1' will be displayed.
5. Set switches at the appropriate positions to display BCD numbers (0-9)

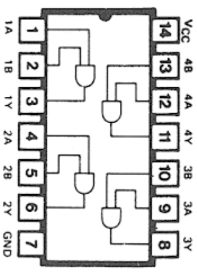
Logic Gates

Logic gates process signals which represent **true** or **false**. Normally, the positive supply voltage +5V represent true and 0V represents false. Other terms which are used for the true and false states are shown in the table. It is best to be familiar with them all.

Logic	**Status**
True	False
1	0
High	Low
ON	OFF
+5 V	0 V

Gates are identified by their function: AND, OR, NOT, NAND, NOR, EX-OR and EX-NOR. Capital letters are normally used to make it clear that the term refers to a logic gate. The basic operations are described below with the aid of truth tables.

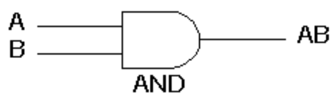
Basic Logic Gates

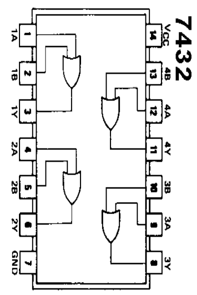


<u>AND Gate</u>

The AND gate is an electronic circuit that gives a **high** output (1) only if **all** its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB.

2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

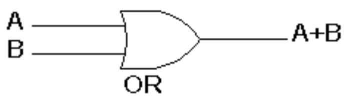


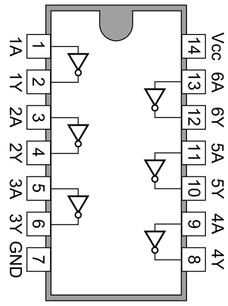


<u>OR Gate</u>

The OR gate is an electronic circuit that gives a high output (1) if **one or more** of its inputs are high. A plus (+) is used to show the OR operation.

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

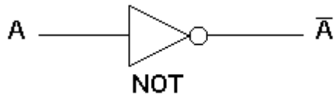




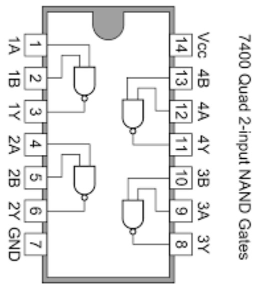
NOT Gate

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an *inverter*. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs.

NOT gate	
A	$\overline{A}$
0	1
1	0



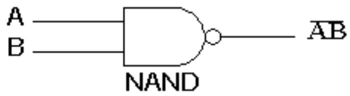
Universal Gates

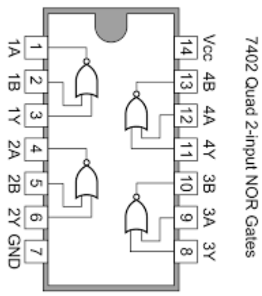


NAND Gate

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

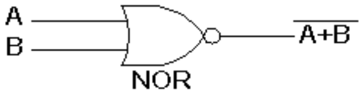


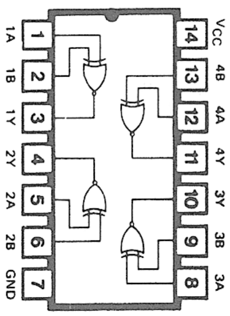


NOR Gate

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if **any** of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

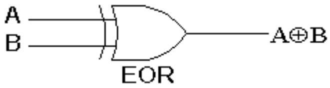


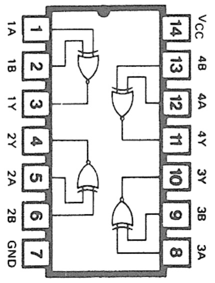


EX-OR or XOR Gate

The '**Exclusive-OR**' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. An encircled plus sign (⊕) is used to show the X-OR operation.

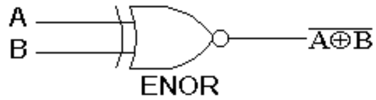
2 Input EXOR gate		
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0





<u>EX-NOR or XNOR Gate</u>

The **'Exclusive-NOR'** gate circuit does the opposite to the X-OR gate. It will give a low output if **either, but not both**, of its two inputs are high. The symbol is an X-OR gate with a small circle on the output. The small circle represents inversion.



2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

Procedure:

1. Connect the logic Trainer to 220V AC power supply.
2. Turn on the Trainer and verify the DC voltage by using voltmeter. Install the IC chip under experiment, on the trainer's breadboard.
3. Connect the +VCC (pin # 14) and Ground (pin # 7) pins of the IC to +5V and Ground supply of the trainer board.
4. Make the appropriate circuit connections as shown in Fig.2.1 Use the trainer's logic switches to provide "0" and "1" at the input and use the trainer's LEDs to display the outputs. Note that there are more than one gates in each IC chip, so you can use any one of these gates to make your connections for the pin numbers corresponding to each gate in that particular chip.
5. Test all the possible combinations of inputs and verify the output according to the truth tables.

Conclusion:

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