HITEC UNIVERSITY
Department of Computer Science and Engineering

BS Computer Science Program (Batch 2016)

Course Code	**EC-121**
Course Title	**Digital Logic Design**
Credit Hours	4 (3+1)
Contact Hours	6 (3+3)
Semester	BSCS 3rd Semester — Fall 2017
Prerequisite	Programming Fundamentals
Course Instructors	Dr Hashim Ali, Ms Sadia Azam
Designation	Assistant Professor, Lecturer
Email	hashim.ali@hitecuni.edu.pk, sadia.azam@hitecuni.edu.pk

Course Objective:

To introduce the basic knowledge of Boolean algebra, design and analysis of Combinational Logic Circuits, design and analysis of Sequential Logic Circuits, Registers, Counters, Memory and programmable logic devices.

Course Outline:

Introduction, number systems, Boolean algebra, logic gates (AND, OR, NOT etc.), Karnaugh maps, QM method, combinational circuits, half & full adder and subtractor, comparator, encoders, decoders, multiplexer, de-multiplexer, sequential circuits, Flip Flop, (RS, JK, D, T, Master Slave), state transition diagram, counters, registers, memories, PLAs, Programmable Logic Devices (PLDs), hardware descriptive language (HDL Verilog), lab assignments using tools such as Verilog HDL/VHDL, Logisim, etc.

Recommended Books:

• M. Morris R. Mano, Michael D. Ciletti, *"Digital Design: With an Introduction to the Verilog HDL"*, 5th edition, Pearson, 2012, ISBN: 978-0132774208.
• Thomas L Floyd, *"Digital Fundamentals"*, 11th edition, Pearson, ISBN-13: 978-0132737968.

Office Hours:

- Friday, 02:00 — 04:00
- Appointment by email

Grading Policy:
75% class attendance is mandatory to appear in the examination.
Course grades will be determined by the following weights:

Theory (70%)		**Laboratory (30%)**	
Assignments	2%	Lab Reports	4%
Quizzes	10%	Lab Performance	10%
Sessional - I	10%	Viva Voce	10%
Sessional - II	10%	Project	6%
Final Exam	38%		
Course Total (100%)	**Theory (75%) + Laboratory (30%)**		

Schedule of Exams:
Commencement of Classes: September 18, 2017
Sessional-I: , 2017
Sessional-II: , 2017
Final Exam: , 2017
Results Notification: , 2017

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BS Computer Science Program (Batch 2016)

EE-203: Digital Logic Design 3 (2+1)
3rd Semester — Fall 2017

Week: Lecture Date	Lecture Breakdown	Evaluation
Week 1: 20/02/17 23/02/17		—
Week 2: 28/02/17 02/03/17		—
Week 3: 07/03/17 09/03/17		Quiz 1
Week 4: 14/03/17 16/03/17		Quiz 2
Week 5: 21/03/17 23/03/17		Quiz 3
Week 6: 28/03/17 30/03/17		Ass 1 - Deadline
Week 7: 03-04/04/17	**Sessional - I Exam**	
Week 8: 11/04/17 13/04/17		—
Week 9: 18/04/17 20/04/17		Quiz 4
Week 10: 25/04/17 27/94/17		Quiz 5
Week 11: 09/05/17 11/05/17		Quiz 6
Week 12: 16/05/17 18/05/17		—
Week 13: 15-19/05/17	**Sessional - II Exam**	
Week 14: 23/05/17 25/05/17		—
Week 15: 30/05/17 01/06/17		Quiz 7
Week 17: 06/06/17		—

08/06/17		
Week 17: 13/06/17 15/06/17		Quiz 8
Week 18: 20/06/17 22/06/17		Ass 2 - Deadline
Week 19: 19-23/06/17	**Final Exam**	